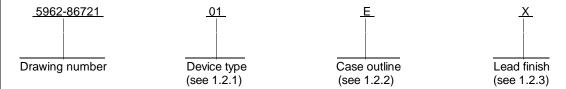
							F	REVISI	IONS										
LTR				D	ESCR	RIPTIO	N					DATE (YR-MO-DA)		DA)	APPROVED				
Α		es to test to 67268.						de ide	nt. no.	from		87	-11-24	ļ		R. P. Evans			
В		neric part	rt number 1691A. Changes to table I. Editorial changes 94-10-05					5		M.	A. Fry	e							
REV		THE (ORIGI	NAL	FIRS	T PA	GE O	F TH	IS DI	RAWII	NG HZ	AS BI	EEN F	REPL#	ACED				
		THE (ORIGI	NAL	FIRS	т ра	GE O	F TH	IS DI	RAWII	NG HZ	AS BE	CEN I	REPL#	ACED				
SHEET		THE (ORIGI	NAL	FIRS	T PA	GE O	F TH	IS DI	RAWII	NG HA	AS BE	CEN F	REPL#	ACED				
SHEET		THE (ORIGI	NAL	FIRS	T PA	GE O	г тн	IS DI	RAWII	NG HZ	AS BE	CEN F	REPLA	ACED				
SHEET REV SHEET REV STATU		THE	ORIGI		FIRS	T PA	GE O	Б ТН	IS DI	RAWII	NG HA	AS BI	B	REPLA B	ACED B	В	В	В	I
SHEET REV SHEET REV STATU		THE		/	FIRS											B 11	B 12	B 13	_
REV SHEET SHEET REV STATU OF SHEETS PMIC N/A		THE	REV SHE	/ EET		B 1	В	В	В	B 5	B 6	B 7	В 8	B 9	B 10	11 PLY (12	13	I
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA MICRO	NDARI	D	REV SHE PREF Dona	/ EET	O BY Osborn	B 1	В	В	В	B 5	B 6	B 7	В 8	B 9	B 10	11 PLY (12	13	_
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA MICRO DR THIS DRAW FOR	NDARI OCIRCU AWING ING IS AVAI USE BY ALL	D UIT 6	REV SHE PREF Dona CHEC D. A	/ PARED ald R. (D BY Osborn BY nzo	B 1	В	В	B 4	B 5	B 6	B 7 SE EL DA	B 8 ECTR YTON	B 9 ONIC:	B 10 S SUP O 454	11 PLY 0	12 CENTE	13	1
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- 1. SCOPE
- 1.1 <u>Scope</u>. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".
 - 1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	Generic number	<u>Circuit function</u>
01	26LS30, 1691A	Dual differential RS-422 party line/quad single ended RS-423 line driver

1.2.2 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
Е	CDIP1-T16 or GDIP2-T16	16	Dual-in-line
F	CDFP3-F16 or GDFP2-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 <u>Lead finish</u>. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V _{CC})	
Supply voltage range (V _{EE})	
Input votage range	-1.5 V dc to +15.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P _D) <u>1</u> /	500 mW
Lead temperature (soldering, 4 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA})	90° C/W
Junction temperature (T _J)	+175° C

1.4 Recommended operating conditions.

EIA RS-422 connection, mode voltage	≤0.76 V
Supply voltage range (V _{CC})	+4.5 V dc to +5.5 V dc
Supply voltage (V _{FF})	GND
Minimum high-level input voltage (V _{IH})	2.0 V dc
Maximum low-level input voltage (V _{II})	0.8 V dc
Ambient operating temperature range (T _A)	-55° C to +125° C
EIA RS-423 connection, mode voltage	≥2.0 V
Supply voltage range (V _{CC})	+4.75 V dc to +5.5 V dc
Supply voltage range (V _{FF})	-4.75 V dc to -5.5 V dc
Minimum high-level input voltage (V _{IH})	2.0 V dc
Maximum low-level input voltage (V _{IL})	0.8 V dc
Ambient operating temperature range (T _A)	-55° C to +125° C
· · · · · · · · · · · · · · · · · · ·	

 $\underline{1'}$ Must withstand the added P_D due to short circuit test (e.g., I_{SA}/I_{SB}).

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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and bulletin</u>. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883

- Test Methods and Procedures for Microelectronics.

MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.
 - 3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.
 - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.
 - 3.2.3 Truth table and logic diagram. The truth table and logic diagram shall be as specified on figure 2.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.5 <u>Marking</u>. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

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	1 7	NDLE I. <u>Electrical</u>	performance chara	deteriones.	1			1
Test	Symbol		Conditions Group A		Device	Limits		Unit
		-55° C ≤ T _A ≤ +125° C sunless otherwise specified		subgroups	type	Min	Max	
EIA RS-422 Connect	t ion , mode voltage	≤0.76 V <u>1</u> / <u>2</u> /						
Differential output voltage	Vo	R _L = Infinity	V _{IN} = 2.0 V	1, 2, 3	01		6.0	V
V _{A, B}	\overline{V}_{O}		V _{IN} = 0.8 V				-6.0	
Differential output voltage	V _T	$R_L = 100\Omega$	V _{IN} = 2.0 V	1, 2, 3	01	2.0		V
V _{A, B}	\overline{v}_T		V _{IN} = 0.8 V			-2.0		
Common mode offset voltage	V _{OS} , V _{OS}	$R_L = 100\Omega$		1, 2, 3	01		3.0	V
Differential in diff'l output voltage	$ V_{T} - V_{T} $	R _L = 100Ω		1, 2, 3	01		0.4	 V
Differential in common mode offset voltage	V _{OS} - V _{OS}	R _L = 100Ω		1, 2, 3	01		0.4	 V
V _T -V _T	V _{SS}	$R_L = 100\Omega$		1, 2, 3	01	4.0		V
Output voltage common mode range	V _{CMR}	V _{enable} = 2.4 V	<u>3</u> /	1, 2, 3	01	±10		V
Output leakage current	I _{XA}	V _{CC} = 0 V	V _{CMR} = 10 V	1, 2, 3	01		100	μA
	I _{XB}		V _{CMR} = -10 V				-100	
Off-state output current (high	I _{OX}	V _{CC} = +5.5 V	V _{CMR} = 10 V	1, 2, 3	01		100	μΑ
impedance)			V _{CMR} = -10 V				-100	

See footnotes at end of table.

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SIZE

A

SIZE

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	TABL	E I. Electrical perforr	mance characteri	istics - continu	ed.				
Test	Symbol	Conditions $-55^{\circ} \text{C} \leq \text{T}_{A} \leq \text{unless otherwise}$	< +125° C	Group A subgroups	Device type	Limits	Max	Unit	
Output short circuit current	I _{SA} , I _{SB}	V _{IN} = 2.4 V V _{CC} = +5.5 V	V _{OB} = 6.0 V	1, 2, 3	01	10	150	mA	
<u>4</u> /			V _{OA} = 0 V			-10	-150		
		V _{IN} = 0.4 V V _{CC} = +5.5 V	V _{OB} = 0 V	1, 2, 3	01	-10	-150		
			V _{OA} = 6.0 V			10	150		
Supply current	lcc	V _{IN} = 0.4 V, V _C	_C = +5.5 V	1, 2, 3	01		30	mA	
Input high voltage	V _{IH}	<u>5</u> /		1, 2, 3	01	2.0		V	
Input low voltage	V _{IL}	<u>5</u> /		1, 2, 3	01		0.8	V	
Input high current	Iн	V _{CC} = +5.5 V	V _{IN} = 2.4 V	1, 2, 3	01		40	μA	
			V _{IN} = 15 V				100		
Input low current	I _{IL}	V _{CC} = +5.5 V	V _{IN} = 0.4 V	1, 2, 3	01		-200	μА	
Input clamp voltage	V _{IC}	I _{IN} = -12 mA, V _O	_{CC} = +4.5 V	1, 2, 3	01		-1.5	V	
Functional tests	FT	See 4.3.1.c		7, 8	01				
Differential output rise and fall time 6/	t _r , t _f	$R_L = 100\Omega, T_A = C_L = 500 \text{ pF}, V_C = 0$ $V_{EE} = 0$	= 25°C, _{CC} = 5.0 V, se figure 3	9	01		250	ns	
Output propagation delay time 6/	t _{PDH} , t _{PDL}	$R_L = 100\Omega, T_A = C_L = 500 \text{ pF}, V_C = GND, Se$	= 25°C, _{CC} = 5.0 V, se figure 3	9	01		200	ns	
Output enable to output time 6/	t _{LZ} , t _{ZH}	$R_L = 100\Omega, T_A = C_L = 500 \text{ pF}, V_C = 0 \text{ pF}, V_{EE}$	= 25°C,	9	01		300	ns	
	t _{HZ} , t _{ZL}	C _C = 0 pF, V _{EE} See figure 3	= GND,				350	-	
See footnotes at end of	f table.			-+	+	+	-	+	
	CTANDARD		SIZE				7		

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Test	Symbol	Conditi	ons	Group A	Device	Limits		Unit
		-55° C <u><</u> T _Δ	-55° C ≤ T _A ≤ +125° C unless otherwise specified		type	Min	Max	
EIA RS-423 conne	ction, mode voltaç	ge ≥2.0 V			'	·	,	
Output voltage	V _O	$\begin{vmatrix} R_{L} = Infinity \\ V_{CC} = V_{EE} = \\ 4.75 \text{ V} \end{vmatrix}$	V _{IN} = 2 V	1, 2	01	4.0 3.9	6.0	V
	\overline{V}_{O}	_ 4.75 V	V _{IN} = 0.4 V	1, 2	01	-4.0	-6.0	-
Output voltage	V _T	$R_L = 450\Omega$,	V _{IN} = 2.4 V	1, 2, 3	01	3.6	-6.0	V
n.	\overline{v}_T	$- V_{CC} = V_{EE} = 4.75 \text{ V}$	V _{IN} = 0.4 V	_		-3.6		-
Output unbalance <u>7</u> /	$ V_{T} - V_{T} $	$R_L = 450\Omega, V_{CC} $	= V _{EE}	1, 2, 3	01		0.4	V
Output leakage power off	I _{X+}	V _{CC} = V _{EE} =	V _{OUT} = 6.0 V	1, 2, 3	01		100	μA
	I _{X-}		V _{OUT} =-6.0 V				-100	
Output short circuit current <u>4</u> /	I _{S+}	V _{OUT} = 0 V, V _{CC} = 5.5 V, V _{EE} = -5.5 V	V _{IN} = 2.4 V	1, 2, 3	01	-20	-150	μA
<u></u>	I _{S-}	VEE0.5 V	V _{IN} = 0.4 V			20	150	
Positive supply current	I _{CC}	$V_{IN} = 0.4 \text{ V}, R_{L} = V_{CC} = V_{EE} = 5$	Infinity 5.5 V	1, 2, 3	01		30	mA
Negative supply current	I _{EE}	$V_{IN} = 0.4 \text{ V}, R_{L} = V_{CC} = V_{EE} = 5$	Infinity 5.5 V	1, 2, 3	01		-22	mA
Input clamp voltage	V _{IC}	I _{IN} = -12 mA, V _{EE} = -5.5 V	V _{CC} = +4.75 V	1, 2, 3	01		-1.5	V
Input high voltage	V _{IH}	9/		1, 2, 3	01	2.0		V
Input low voltage	V _{IL}	<u>9</u> /		1, 2, 3	01		0.8	V
See footnotes at end o	f table.							
MICR	STANDARD OCIRCUIT DRAV	VING	SIZE A				5962-	-86721
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	TABL	E I. Electrical perfo	rmance characteris	tics - continu	ed.			
Test	Symbol		Conditions			Limits		Unit
		-55° C ≤ T _A ≤ +125° C sunless otherwise specified		subgroups	type	Min	Max	
Input high current	I _{IH}	V _{CC} = V _{EE} = V _{IN} = 2.4 V	$ V_{CC} = V_{EE} = 5.5 \text{ V},$ $V_{IN} = 2.4 \text{ V}$		01		40	μA
		V _{CC} = 5.5 V, V _{IN} = 15 V, V _{EE} = -5.0 V					100	
Input low current	I₁∟	$ V_{CC} = V_{EE} = 5.5 \text{ V},$ $V_{IN} = 0.4 \text{ V}$		1, 2, 3	01		-200	μА
Functional tests	FT	See paragraph 4	See paragraph 4.3.1.c		01			
Rise and fall time	t _r , t _f	$R_L = 450\Omega$, $C_L = 500 \text{ pF}$, $C_C = 0 \text{ pF}$, See figure 3	T _A = 25° C, V _{CC} = 5.0 V, V _{EE} = -5.0 V	9	01		300	ns
			V _{CC} =+4.75 V to +5.5 V V _{EE} =-4.75 V to -5.5 V	10, 11 <u>6</u> /			375	
Output propagation delay time	t _{PDH} , t _{PDL}	$R_L = 450\Omega$, $C_L = 500 \text{ pF}$, $C_C = 0 \text{ pF}$, See figure 3	$T_{A} = 450\Omega,$ $T_{A} = 25^{\circ} C,$ $V_{CC} = 5.0 V,$ $V_{FF} = -5.0 V$		01		300	ns
			V _{CC} =+4.75 V to +5.5 V V _{EE} =-4.75 V to -5.5 V	10, 11 <u>6</u> /			375	

- $\underline{1}/\ R_L$ connected between each output and its complement.

- 2/ Measurements for ATE loads are for single-ended conditions.
 3/ V_{CMR} is guaranteed by tested parameters I_{XA}, I_{XB} and I_{OX}.
 4/ Not more than one output should be shorted at a time. Duration of short circuit test should not exceed one second.
- 5/ Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.
- 6/ This parameter is guaranteed, but not tested.
- 7/ This parameter is tested by forcing an equivalent current.
- 8/ The V_{IC} parameter in the RS423 mode is guaranteed by the tested V_{IC} parameter in the RS422 mode.
- 9/ Input thresholds are tested during DC tests and may be done in combination with testing of other DC parameters.

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Device type	01	
Case outline	E, F	2
Terminal number	Terminal s	symbol
1	V _{CC}	NC
2	INPUT A	V _{CC}
3	INPUT/ENABLE B	INPUT A
4	MODE	INPUT/ENABLE B
5	GND	MODE
6	INPUT/ENABLE C	NC
7	INPUT D	GND
8	V _{EE}	INPUT/ENABLE C
9	SLEW RATE CONTROL D	INPUT D
10	OUTPUT D	V _{EE}
11	OUTPUT C	NC
12	SLEW RATE CONTROL C	SLEW RATE CONTROL D
13	SLEW RATE CONTROL B	OUTPUT D
14	OUTPUT B	OUTPUT C
15	OUTPUT A	SLEW RATE CONTROL C
16	SLEW RATE CONTROL A	NC
17		SLEW RATE CONTROL B
18		OUTPUT B
19		OUTPUT A
20		SLEW RATE CONTROL A

FIGURE 1. <u>Terminal connections</u>.

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	Inputs		Out	tputs
Mode	A(D)	B(C)		
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

0 = low level1 = high levelZ = high impedance

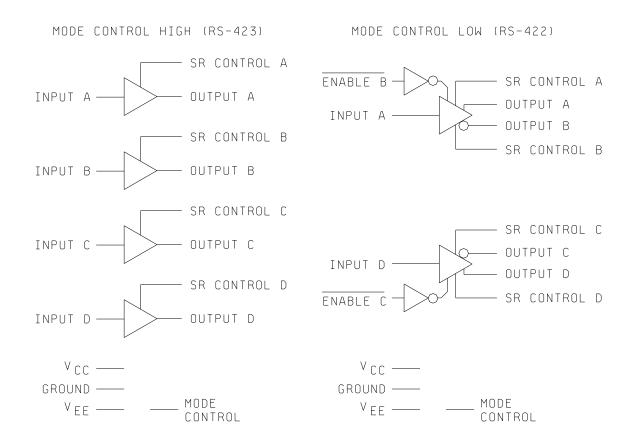
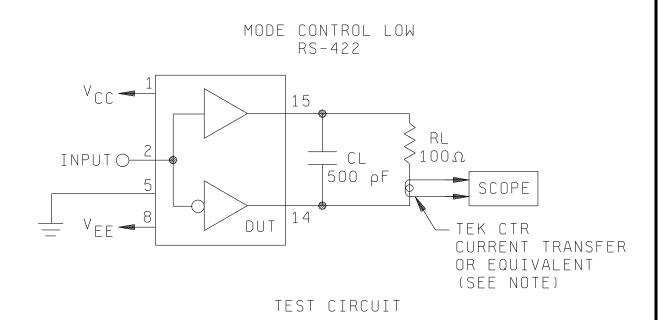
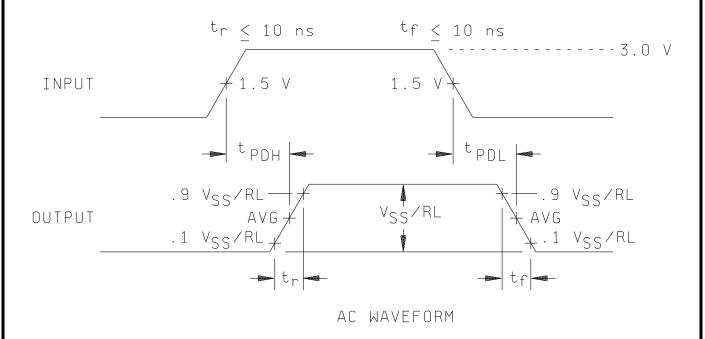


FIGURE 2. Truth table and logic diagram.

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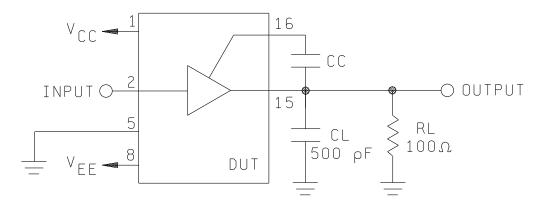


NOTE: Current probe is the easiest way to display a differential waveform.

FIGURE 3. AC test circuits and waveforms.

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MODE CONTROL HIGH RS-422



TEST CIRCUIT

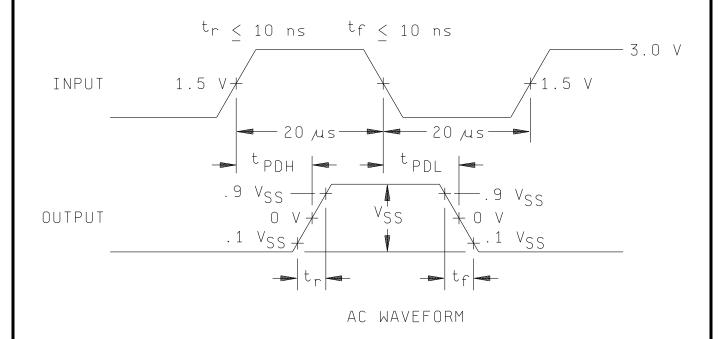
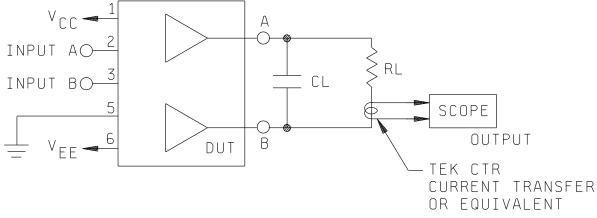


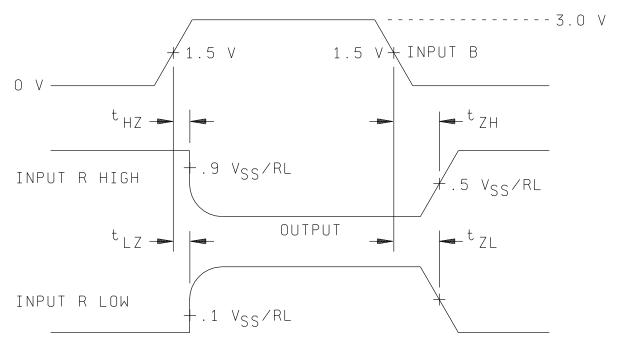
FIGURE 3. AC test circuits and waveforms - continued.

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TEST CIRCUIT



AC WAVEFORM

FIGURE 3. AC test circuits and waveforms - continued.

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- 3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change</u>. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.9 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
 - 4. QUALITY ASSURANCE PROVISIONS
 - 4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ} C$, minimum.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
 - 4.3.1 Group A inspection.
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
 - c. Subgroups 7 and 8 shall include verification of the truth table.
 - 4.3.2 Groups C and D inspections.
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition A, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ} C$, minimum.
 - Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

^{*} PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.
- 6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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^{**} Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-10-05

Approved sources of supply for SMD 5962-86721 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN <u>1</u> /
5962-8672101EX	27014	DS1691AJ/883
5962-8672101FX	<u>2</u> /	AM26LS30/BFA
5962-86721012X	<u>2</u> /	AM26LS30/B2C

- 1/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 2/ No longer available from an approved source.

Vendor CAGEVendor namenumberand address

27014 National Semiconductor 2900 Semiconductor Drive

P.O. Box 58090

Santa Clara, CA 95052-8090

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.